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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/081,840	Applicant(s) LEWIS, TIMOTHY A.
	Examiner Thomas J. Cleary	Art Unit 2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☒ Claim(s) *2 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *20 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,684,997 to Kau et al. ("Kau"), US Patent Number 6,093,213 to Favor et al. ("Favor"), and knowledge commonly known in the art, as evidenced by the Microsoft Press Computer Dictionary, 3rd Edition ("Microsoft").

2. In reference to Claim 1, Kau teaches a real-time clock (See Column 132 Lines 22-50); a register file containing one or more timing sensitive registers (See Column 2 Lines 22-50); an update-in-progress status bit that determines a certain fixed period of time for which the timing sensitive registers are valid (See Column 133 Lines 9-13); and an SMI routine that determines if an update cycle is taking place, if one is taking place, the SMI routine writes the index of a control register to a second register location, reads the control register to determine if an update-in-progress (UIP) bit is set, and repeats the previous two steps if the UIP is not set, and if one is not taking place, the SMI

routine exits (See Column 132 Lines 29-32 and Column 133 Lines 11-23). Kau does not teach a retriggerable, fixed duration timer that is triggered by reads of zero from the update-in-progress status bit; a latch that is set if the timer is running when a system management interrupt is asserted and cleared when SMI is deasserted; means for reading the output status of the latch; a timer that is triggered by reading zero from a first register location; and a status latch for storing the status of the timer, which status is read using a status bit. Kau further teaches that an operation to read or write information to the real-time clock should take no longer than 244 μs (See Column 133 Lines 20-23). Official Notice is taken that the use of a timer for measuring time intervals is well known in the art, as evidenced by Microsoft (See entry 'timer'), and one of ordinary skill in the art would use a timer to provide an indication of how much time is remaining to perform the read or write operation. Favor teaches a register (See Figure 10 Number 988), which is equivalent to both a latch and a status latch, which is set if an SMI is not running when another SMI is asserted and cleared when the another SMI is deasserted (See Column 34 Lines 59-67); and a status bit for reading the output status of the register (See Figure 10 Number 970).

It would have been obvious to one or ordinary skill in the art at the time the invention was made to combine the device of Kau with the timer commonly known in the art and the register use of Favor, resulting in the invention of Claim 1, because Kau teaches that the UIP bit is asserted 244 μs prior to the start of an update cycle and an operation to read or write information to the real-time clock should take no longer than 244 μs (See Column 133 Lines 11-23 of Kau), and thus a timer would be an obvious

choice for measuring the 244 μs time available to read or write the information (See entry 'timer' in Microsoft); and to prevent an SMI from being received when the processor is processing another SMI (See Column 34 Lines 59-62 of Favor).

3. In reference to Claim 2, Kau, Favor, and Microsoft teach the limitations as applied to Claim 1 above. Kau further teaches that writing to the second register location is writing 0A to I/O location 0x70, reading a third register location is reading I/O location 0x71, and repeating the previous two steps until the value of bit 7 of I/O location 0x71 is not set (See Column 132 Lines 29-54).

It would have been obvious to one or ordinary skill in the art at the time the invention was made to combine the device of Kau with the timer commonly known in the art and the register use of Favor, resulting in the invention of Claim 2, because Kau teaches that the UIP bit is asserted 244 μs prior to the start of an update cycle and an operation to read or write information to the real-time clock should take no longer than 244 μs (See Column 133 Lines 11-23 of Kau), and thus a timer would be an obvious choice for measuring the 244 μs time available to read or write the information (See entry 'timer' in Microsoft); and to prevent an SMI from being received when the processor is processing another SMI (See Column 34 Lines 59-62 of Favor).

4. Claims 3, 4, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kau and Favor.

5. In reference to Claim 3, Kau teaches system having timing-sensitive registers and a plurality of I/O locations, and a method comprising the steps of: writing to a first I/O location; reading a second I/O location; if a predetermined bit of the value that is read from the second I/O location is set, repeating previous two steps until the predetermined bit of the read value is not set; and stopping the method (See Column 132 Lines 29-32 and Column 133 Lines 11-23). Kau does not teach a status latch; reading the status latch; and stopping if the status latch is zero. Favor teaches a status latch (See Figure 10 Number 988) and stopping when a read of the status latch returns a result of zero (See Column 34 Lines 46-67).

It would have been obvious to one or ordinary skill in the art at the time the invention was made to combine the device of Kau with the register use of Favor, resulting in the invention of Claim 3, in order to prevent an SMI from being received when the processor is processing another SMI (See Column 34 Lines 59-62 of Favor).

6. In reference to Claim 4, Kau and Favor teach the limitations as applied to Claim 3 above. Kau further teaches that writing to a first I/O location is writing 0A to I/O location 0x70, reading a second I/O location is reading I/O location 0x71, and repeating the previous two steps until the value of bit 7 of I/O location 0x71 is not set (See Column 132 Lines 29-54).

It would have been obvious to one or ordinary skill in the art at the time the invention was made to combine the device of Kau with the register use of Favor,

resulting in the invention of Claim 4, in order to prevent an SMI from being received when the processor is processing another SMI (See Column 34 Lines 59-62 of Favor).

7. In reference to Claim 5, Kau teaches system having timing-sensitive registers and a plurality of I/O locations, and a method comprising the steps of: software that writes to a first I/O location; software that reads from a second I/O location; software that, if a predetermined bit of the value that is read from the second I/O location is set, repeats previous two steps until the predetermined bit of the read value is not set; and software that exits when the predetermined bit of the read value is not set to zero (See Column 132 Lines 29-32 and Column 133 Lines 11-23). Kau does not teach a status latch; a code segment that reads the status latch; and a code segment that exits if the status latch is zero. Favor teaches a status latch (See Figure 10 Number 988) and exiting when a read of the status latch returns a result of zero (See Column 34 Lines 46-67).

It would have been obvious to one or ordinary skill in the art at the time the invention was made to combine the device of Kau with the register use of Favor, resulting in the invention of Claim 5, in order to prevent an SMI from being received when the processor is processing another SMI (See Column 34 Lines 59-62 of Favor).

8. In reference to Claim 6, Kau and Favor teach the limitations as applied to Claim 5 above. Kau further teaches that writing to a first I/O location is writing 0A to I/O location 0x70, reading a second I/O location is reading I/O location 0x71, and repeating the

previous two steps until the value of bit 7 of I/O location 0x71 is not set (See Column 132 Lines 29-54).

It would have been obvious to one or ordinary skill in the art at the time the invention was made to combine the device of Kau with the register use of Favor, resulting in the invention of Claim 6, in order to prevent an SMI from being received when the processor is processing another SMI (See Column 34 Lines 59-62 of Favor).

Claim Objections

9. Claim 2 is objected to because of the following informalities: the phrase "O location 0x71" appears to have been used in place of the phrase "I/O location 0x71" in Line 4. The Examiner will assume usage of the phrase "I/O location 0x71" for the purposes of evaluating prior art. Appropriate correction, if necessary, is required.

10. Claim 6 is objected to because of the following informalities: Claim 6, directed towards software, is dependent on Claim 2, directed towards a system. Based on the dependencies of Claims 2 and 4, which contain language similar to Claim 6, the Examiner will assume Claim 6 is dependent on Claim 5 for the purposes of evaluating prior art. Appropriate correction is required.

Drawings

11. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figure 2 Number 36.

12. Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

13. The disclosure is objected to because of the following informalities: on Page 3 Line 25, the phrase "timer 15 timer 15" appears to have been used in place of the phrase "timer 15" and on Page 4 Line 20, the phrase "244 μ4s" appears to have been used in place of the phrase "244 μs". Appropriate correction, if necessary, is required.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The Examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

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